Von Braun Microelectronics Design Center

Wernher von Braun
centro de pesquisas avançadas

Asic Designs

Werhner von Braun microelectronics has a team of engineers experienced in high-speed digital design; we deliver custom chip designs targeted for special-purpose devices resulting on Application Specific Integrated Circuits (ASICs). In consequence, our process enables clients to achieve their time-to-market goals minimizing the time necessary to meet the critical design verification stages.

Our Design Center starts its ASIC design processes with well written system specification requirement documentation and a detailed hardware&software identify-implementation-specification “I2S™ von Braun’s process”. We can start design with customer written specs, or we can write whole specifications to meet customer’s project requirements.

Writing the specifications or using mathematical methods helps our experienced teams efficiently in detect errors on important aspects to the success of the project. The importance of “Offline-Checking” can also easily identify missing or spurious informations, helping schedules and costs definitions to be agreed upon our interface and verification plan by von Braun’s customer.

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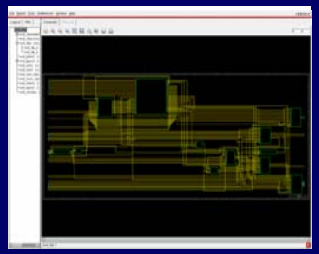

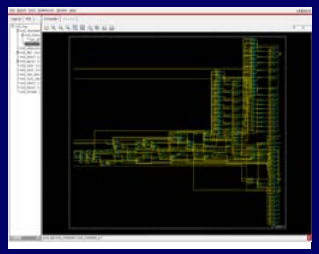

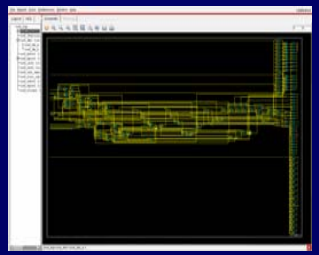

Our Language - Verilog and VHDL Expertise

Our designers have considerable expertise in both languages using top down methodology design we transform ideas from the abstract into a physical form that can be synthesizable built and implemented.
The Design Center has experience in the use of the Verilog and VHDL made available by Cadence Design Systems, and FPGA programmable tools.

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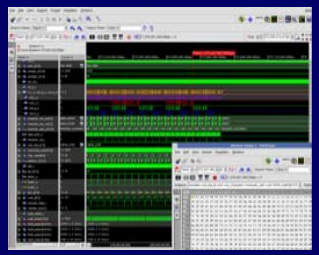

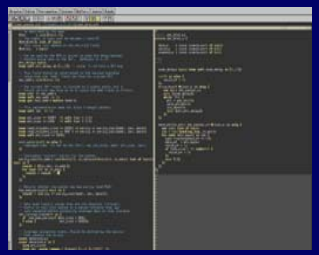

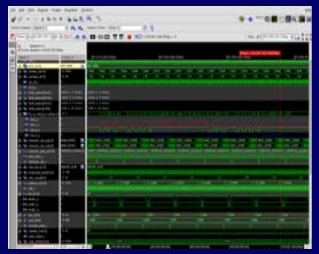

Verification Services

Customer's requirement specifications are captured into a system level detail to search for many issues as possible at the block level to make sure that fits into the intended design by the entire verification team.

- We provide the following services:
- Architectural design types of IP blocks
- Verification environment, block level verification.
- Test plan specification.
- Lint Checking
- Formal mode checking
- Code and Functional verification, coverage analysis
- Protocol checking and enhancing existing environments.
- Directed Random Testing
- Brainstorm and consulting in the process of selecting the right verification tools for the existing environment.
- Scheduling and estimating the required efforts.
- Hardware Simulation acceleration

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FPGA Services

The development of projects using today's FPGA is complex such as ASIC designs, though may be called as SOC "system-on-chip", it is usually part of great systems with other ASICs and chips.
Werhner von Braun has also been specialized in large gate count designs, high clock data rate designs and Netcom system architecture considerations (Wireless, PDH, SDH/ATM, Gigabit-Ethernet and Frame Relay).
Using our ASIC based process, the engineers team implements the design to create a high-quality, efficient design that works on both devices, FPGA or ASICs.
The creation of our designs meets speed and power requirements, since our IP core has been ported to an ASIC; this quality can be optimized resulting on higher yield ASIC products.
Time-to-market has some significant cost savings and schedule for our customers. FPGA companies have early access to the newest technology; in this case, FPGA becomes the preferred architecture for system-on-chip designs

- High density volume design the tested under FPGA technology,
- Faster prototyping and prove of concept hardware,
- A design to be ported to ASIC since market justifies it.

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Our core competencies include:

- Cadence Design Systems (Synthesis and Verification tools)
- Programmable Logic – FPGA, CPLD, PAL
- Custom DSP projects
- Golden models prove of concept design
- Simulation services

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